In the Claims:

1. (Original) A method of fabricating a transistor, the method comprising:

providing a workpiece;

growing a stressed semiconductor layer over the workpiece;

growing a first layer of silicon and carbon over the stressed semiconductor layer;

depositing a gate dielectric material over the layer of silicon and carbon;

depositing a gate material over the gate dielectric material;

patterning the gate material and gate dielectric material to form a gate and a gate dielectric disposed over the layer of silicon and carbon; and

forming a source region and a drain region in the layer of silicon and carbon and stressed semiconductor layer, wherein the source region, drain region, gate, and gate dielectric comprise a transistor.

2. (Original) The method according to Claim 1, wherein growing the layer of silicon and carbon comprises epitaxially growing a layer of about 90 to 99.5% silicon and about 0.5 to 10 % carbon having a thickness of about a few tens of Å to about 5 μm.

3. (Original) The method according to Claim 1, wherein growing the stressed semiconductor layer comprises epitaxially growing a second layer of silicon and carbon, a layer of silicon and germanium, or a layer of silicon, carbon and germanium, and wherein growing the stressed semiconductor layer comprises growing a material having a thickness of about 100 Å to about 5 μm.

4. (Original) The method according to Claim 1, wherein depositing the gate dielectric material comprises depositing a high k dielectric material or an oxide, and wherein depositing the gate material comprises depositing a semiconductor material or a metal.

5. (Currently Amended) The method according to Claim 1, further comprising depositing a [[thin]] semiconductor material over the first layer of silicon and carbon, before depositing the gate dielectric material.

6. (Original) The method according to Claim 5, wherein depositing the thin semiconductor material comprises depositing about 100 Å or less of Si, Ge, SiGe, a bilayer of Si/SiGe, or a bilayer of Ge/SiGe.

7. (Original) The method according to Claim 1, further comprising forming isolation regions in the workpiece, before or after growing the stressed semiconductor layer over the workpiece and growing a first layer of silicon and carbon over the workpiece, and further comprising forming spacers over sidewalls of the gate and gate dielectric.

8. (Original) The method according to Claim 1, wherein providing the workpiece comprises providing a silicon-on-insulator (SOI) wafer.

9. (Currently Amended) A method of fabricating a transistor, the method comprising:

providing a workpiece;

~~growing~~ forming a first layer of silicon and carbon over the workpiece;

depositing a gate dielectric material ~~over~~ directly on the layer of silicon and carbon~~, the~~

~~gate dielectric comprising a high dielectric constant (k) material~~;

depositing a gate material over the gate dielectric material~~, the gate material comprising a metal~~;

patterning the gate material and gate dielectric material to form a gate and a gate dielectric disposed over the layer of silicon and carbon; and

forming a source region and a drain region in at least the layer of silicon and carbon, wherein the source region, drain region, gate, and gate dielectric comprise a transistor.

10. (Currently Amended) The method according to Claim 9, wherein ~~growing~~ forming the layer of silicon and carbon comprises epitaxially growing a layer of about 90 to 99.5% silicon and about 0.5 to 10 % carbon having a thickness of about a few tens of Å to about 5 μm.

11. (Currently Amended) The method according to Claim 9, further comprising ~~growing~~ forming a stressed semiconductor layer over the workpiece, before ~~growing~~ forming the first layer of silicon and carbon over the workpiece, wherein forming the source region and the drain region comprises forming the source region and the drain region in the stressed semiconductor layer.

12. (Currently Amended) The method according to Claim 11, wherein ~~growing~~ forming the stressed semiconductor layer comprises epitaxially growing a second layer of silicon and carbon, a layer of silicon and germanium, or a layer of silicon, carbon and germanium~~, and wherein growing the stressed semiconductor layer comprises growing a material having a thickness of about 100 Å to 5 μm~~.

13. (Currently Amended) The method according to Claim [[9]] 40, further comprising depositing a thin semiconductor material over the first layer of silicon and carbon, before depositing the gate dielectric material.

14. (Original) The method according to Claim 13, wherein depositing the thin semiconductor material comprises depositing about 100 Å or less of Si, Ge, SiGe, a bilayer of Si/SiGe, or a bilayer of Ge/SiGe.

15. (Currently Amended) The method according to Claim [[9]] 11, further comprising forming isolation regions in the workpiece, before or after ~~growing~~ forming the stressed semiconductor layer over the workpiece and ~~growing~~ forming a first layer of silicon and carbon over the workpiece~~, and further comprising forming spacers over sidewalls of the gate and gate dielectric~~.

16. (Original) The method according to Claim 9, wherein providing the workpiece comprises providing a silicon-on-insulator (SOI) wafer.

17-32. (Canceled)

33. (New) The method according to claim 9, wherein the gate dielectric comprises a high dielectric constant (k) material.

34. (New) The method according to claim 33, wherein depositing a gate material over the gate dielectric material comprises depositing a gate material that comprises a metal.

35. (New) The method according to claim 12, wherein growing the stressed semiconductor layer comprises growing a material having a thickness of about 100 Å to 5 μm.

36. (New) The method according to claim 9, wherein forming a first layer of silicon and carbon over the workpiece comprises growing a first layer of silicon and carbon over the workpiece.

37. (New) The method according to claim 9, further comprising forming spacers over sidewalls of the gate and gate dielectric.

38. (New) The method according to Claim 15, wherein the isolation regions are formed before forming the stressed semiconductor layer and forming the first layer of silicon and carbon over the workpiece.

39. (New) The method according to Claim 9, further comprising growing a semiconductor layer over the workpiece, before forming the first layer of silicon and carbon over the workpiece, wherein forming the source region and the drain region comprises forming the source region and the drain region in the stressed semiconductor layer.

40. (New) A method of fabricating a transistor, the method comprising:

providing a workpiece;

epitaxially growing a layer of semiconductor material over the workpiece, the semiconductor material comprising silicon and carbon, silicon and germanium, or silicon, carbon and germanium;

forming a layer of silicon and carbon over the layer of semiconductor material;

depositing a gate dielectric material over the layer of silicon and carbon;

depositing a gate material over the gate dielectric material;

patterning the gate material and gate dielectric material to form a gate and a gate dielectric disposed over the layer of silicon and carbon; and

forming a source region and a drain region in the layer of silicon and carbon and stressed semiconductor layer, wherein the source region, drain region, gate, and gate dielectric comprise a transistor.

41. (New) The method of claim 40, wherein epitaxially growing a layer of semiconductor material comprises epitaxially growing a stressed layer of semiconductor material.

42. (New) The method of claim 40, wherein forming a layer of silicon and carbon comprises epitaxially growing a layer that includes silicon and carbon.

43. (New) The method of claim 40, wherein the layer of silicon and carbon includes about 90 to 99.5% silicon and about 0.5 to 10 % carbon.

44. (New) The method of claim 40, wherein the layer of silicon and carbon has a thickness of about a few tens of Å to about 5 μm.